

## WHAT IS CLAIMED IS:

1           1. An apparatus for designing a memory for use in an  
2 embedded processing system comprising:

3               a simulation controller capable of simulating execution  
4 of a test program to be executed by said embedded processing  
5 system;

6               a memory access monitor capable of monitoring memory  
7 accesses to a simulated memory space during said simulated  
8 execution of said test program, wherein said memory access monitor  
9 is capable of generating memory usage statistical data associated  
10 with said monitored memory accesses; and

11              a memory optimization controller capable of comparing  
12 said memory usage statistical data and one or more predetermined  
13 design criteria associated with said embedded processing system  
14 and, in response to said comparison, determining at least one  
15 memory configuration capable of satisfying said one or more  
16 predetermined design criteria.

1           2.    The apparatus as set forth in Claim 1 wherein said at  
2    least one memory configuration is determined from a predetermined  
3    set of memory types, said predetermined set of memory types  
4    comprising at least two of static random access memory (SRAM),  
5    dynamic random access memory (DRAM), read-only memory (ROM), flash  
6    RAM (FLASH), and electronically erasable programmable read-only  
7    memory (EEPROM).

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1           5. The apparatus as set forth in Claim 1 wherein said  
2 simulation controller simulates execution of said test program  
3 N times and wherein said memory access monitor monitors said memory  
4 accesses during said N simulated executions of said test program  
5 and generates said memory usage statistical data based on said N  
6 simulated executions of said test program.

1           6. The apparatus as set forth in Claim 1 wherein said memory  
2 optimization controller is further capable of determining at least  
3 one figure of merit associated with said at least one memory  
4 configuration, wherein said at least one figure of merit indicates  
5 a degree to which said at least one memory configuration satisfies  
6 said one or more predetermined design criteria.

1           7. The apparatus as set forth in Claim 1 further comprising  
2 a code optimization controller capable of modifying said test  
3 program in response to said comparison of said memory usage  
4 statistical data and said one or more predetermined design criteria  
5 to thereby enable said embedded processing system to execute said  
6 test program according to said one or more predetermined design  
7 criteria.

1           8.    A method of designing an embedded processing system, the  
2 method comprising the steps of:

3                simulating execution of a test program to be executed by  
4 the embedded processing system;

5                monitoring memory accesses to a simulated memory space  
6 during the simulated execution of the test program;

7                generating memory usage statistical data associated with  
8 the monitored memory accesses;

9                comparing the memory usage statistical data and one or  
10 more predetermined design criteria associated with the embedded  
11 processing system; and

12               in response to the comparison, determining at least one  
13 memory configuration capable of satisfying the one or more  
14 predetermined design criteria.

15           9.    The method as set forth in Claim 8 wherein the at least  
16 one memory configuration is determined from a predetermined set of  
17 memory types, the predetermined set of memory types comprising at  
18 least two of static random access memory (SRAM), dynamic random  
19 access memory (DRAM), read-only memory (ROM), flash RAM (FLASH),  
20 and electronically erasable programmable read-only memory (EEPROM).

1           10. The method as set forth in Claim 9 wherein the at least  
2 one memory configuration comprises a first memory type and a first  
3 memory size associated with the first memory type.

1           11. The method as set forth in Claim 10 wherein the at least  
2 one memory configuration further comprises a second memory type and  
3 a second memory size associated with the second memory type.

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1           12. The method as set forth in Claim 8 wherein the step of  
2 simulating execution of the test program comprises the sub-steps of  
3 simulating execution of the test program N times, wherein the step  
4 of monitoring the memory accesses comprises the sub-steps of  
5 monitoring the memory accesses during the N simulated executions of  
6 the test program, and wherein the step of generating the memory  
7 usage statistical data is based on the N simulated executions of  
8 the test program.

1           13. The method as set forth in Claim 8 further comprising the  
2           step of determining at least one figure of merit associated with  
3           the at least one memory configuration, wherein the at least one  
4           figure of merit indicates a degree to which the at least one memory  
5           configuration satisfies the one or more predetermined design  
6           criteria.

1           14. The method as set forth in Claim 8 further comprising the  
2           step of modifying the test program in response to the comparison of  
3           the memory usage statistical data and the one or more predetermined  
4           design criteria to thereby enable the embedded processing system to  
5           execute the test program according to the one or more predetermined  
6           design criteria.

1 15. An embedded processing system designed according to the  
2 method as set forth in Claim 8.

1 16. An embedded processing system designed according to the  
2 method as set forth in Claim 9.

1 17. An embedded processing system designed according to the  
2 method as set forth in Claim 10.

1 18. An embedded processing system designed according to the  
2 method as set forth in Claim 11.

1 19. An embedded processing system designed according to the  
2 method as set forth in Claim 12.

1 20. An embedded processing system designed according to the  
2 method as set forth in Claim 13.

1 21. An embedded processing system designed according to the  
2 method as set forth in Claim 14.

1           22. For use in a processing system, a computer-readable  
2 storage medium containing computer-executable instructions for  
3 designing a memory for use in an embedded processing system, the  
4 computer-executable instructions comprising the steps of:

5           simulating execution of a test program to be executed by  
6 the embedded processing system;

7           monitoring memory accesses to a simulated memory space  
8 during the simulated execution of the test program;

9           generating memory usage statistical data associated with  
10 the monitored memory accesses;

11           comparing the memory usage statistical data and one or  
12 more predetermined design criteria associated with the embedded  
13 processing system; and

14           in response to the comparison, determining at least one  
15 memory configuration capable of satisfying the one or more  
16 predetermined design criteria.



1           23. The computer-readable storage medium as set forth in  
2 Claim 22 wherein the at least one memory configuration is  
3 determined from a predetermined set of memory types, the  
4 predetermined set of memory types comprising at least two of static  
5 random access memory (SRAM), dynamic random access memory (DRAM),  
6 read-only memory (ROM), flash RAM (FLASH), and electronically  
7 erasable programmable read-only memory (EEPROM).

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1           26. The computer-readable storage medium as set forth in  
2 Claim 22 wherein the step of simulating execution of the test  
3 program comprises the sub-steps of simulating execution of the test  
4 program N times, wherein the step of monitoring the memory accesses  
5 comprises the sub-steps of monitoring the memory accesses during  
6 the N simulated executions of the test program, and wherein the  
7 step of generating the memory usage statistical data is based on  
8 the N simulated executions of the test program.

27. The computer-readable storage medium as set forth in  
Claim 22 further comprising the step of determining at least one  
figure of merit associated with the at least one memory  
configuration, wherein the at least one figure of merit indicates  
a degree to which the at least one memory configuration satisfies  
the one or more predetermined design criteria.

1           28. The computer-readable storage medium as set forth in  
2    Claim 22 further comprising the step of modifying the test program  
3    ~~in response to the comparison of the memory usage statistical data~~  
4    and the one or more predetermined design criteria to thereby enable  
5    the embedded processing system to execute the test program  
6    according to the one or more predetermined design criteria.